REMARKS

Claims 1-15 are present in this application. Claims 1, 3, 5, and 8 are independent.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 3, 4, 6, 7, 9, and 12 are allowed.

Claim Rejection – 35 U.S.C. § 112, first paragraph

Claims 1, 2, 5, 8, 10, 11, and 13-15 have been rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In particular, the Office Action states that the specification as filed does not teach the limitation "with respect to one of said plurality of generated clocks," as recited in claims 1, 5, and 8. Applicant provides the following explanation of the teachings in the present application. In addition, claims 1, 5, and 8 have been amended to clarify that the detection circuit operates with respect to a clock generated by a delay circuit of the polyphase clock generation circuit that delays the input clock.

According to the present specification, the polyphase clock generation circuit 100 comprises a plurality of delay circuits 201 to 208 (page 16, lines 20-22). One of the delay circuits of the polyphase clock generation circuit generates a clock 0 by delaying the input clock (page 17, lines 10-12). The clock 0 is input to a delay circuit 202, and subsequently clocks 1 to 7 are generated (page 17, lines 12-14). Thus, it can be seen that the specification discloses that the clocks, e.g. 1-7, are generated based on the input clock.

Furthermore, according to the present specification, the detection circuit detects which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit. The specification discloses that the detection circuit 110 is constructed from D flip-flops 210 to 216 (page 17, lines 2-3). The detection circuit determines the number of clocks (i.e., integral multiple of a clock cycle) generated by the polyphase clock generation circuit to make a phase shift of the input clock cycle (page 17, lines 15-17). For example, as shown in Figs. 3 and 4, the cycle where 1 turns to 0 for the first time (i.e., as seen in Fig. 3, where the phase of a clock is high and a subsequent clock is low, with respect to clock 0) is between Q4 and Q5. Thus, the phase shift amount of the polyphase clock is detected as clock Q4, and the detection is based on the phase of each clock with respect to clock 0 (e.g., values shown in Fig. 4 are obtained from clock phase relative to clock 0; shown as vertical lines extending from clock 0 in Fig. 3).

As explained above, Applicant submits that the specification does teach all limitations recited in the claims. Applicant requests that the rejection be reconsidered and withdrawn.

Conclusion

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No.

48,222) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: September 15, 2005

Respectfully submitted,

Catherine M. Voskuil
Reg. #: 52,327

By _____
for Charles Gorenstein
Registration No.: 29,271
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Rd
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

RWD
CG/RWD/slb